

(1390 REV. 5-93) US DEPT. OF COMMERCE PATENT & TRADEMARK OFFICE  <div style="text-align: center;"> <b>TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371</b> </div>		ATTORNEY'S DOCKET NUMBER 109716  U.S. APPLICATION NO. (if known, sec 37 C.F.R.1.5)  <div style="text-align: center; font-size: 1.5em;">09/857569</div>
INTERNATIONAL APPLICATION NO. PCT/JP00/06795	INTERNATIONAL FILING DATE September 29, 2000	PRIORITY DATE CLAIMED October 14, 1999
TITLE OF INVENTION METHOD FOR PRODUCING BONDING WAFER AND BONDING WAFER		
APPLICANT(S) FOR DO/EO/US Masatake NAKANO, Kiyoshi MITANI and Shinichi TOMIZAWA		
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:		
<ol style="list-style-type: none"> <li>1. <input checked="" type="checkbox"/> This is a <b>FIRST</b> submission of items concerning a filing under 35 U.S.C. 371.</li> <li>2. <input type="checkbox"/> This is a <b>SECOND</b> or <b>SUBSEQUENT</b> submission of items concerning a filing under 35 U.S.C. 371.</li> <li>3. <input checked="" type="checkbox"/> This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).</li> <li>4. <input type="checkbox"/> A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.</li> <li>5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(c)(2))               <ol style="list-style-type: none"> <li>a. <input type="checkbox"/> is transmitted herewith (required only if not transmitted by the International Bureau).</li> <li>b. <input checked="" type="checkbox"/> has been transmitted by the International Bureau.</li> <li>c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US)</li> </ol> </li> <li>6. <input checked="" type="checkbox"/> A translation of the International Application into English (35 U.S.C. 371(c)(2)).</li> <li>7. <input type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))               <ol style="list-style-type: none"> <li>a. <input type="checkbox"/> are transmitted herewith (required only if not transmitted by the International Bureau).</li> <li>b. <input type="checkbox"/> have been transmitted by the International Bureau.</li> <li>c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired.</li> <li>d. <input type="checkbox"/> have not been made and will not be made.</li> </ol> </li> <li>8. <input type="checkbox"/> A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).</li> <li>9. <input checked="" type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).</li> <li>10. <input type="checkbox"/> A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).</li> </ol>		
<b>Items 11. to 16. below concern other document(s) or information included:</b>		
<ol style="list-style-type: none"> <li>11. <input checked="" type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98.</li> <li>12. <input checked="" type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.</li> <li>13. <input checked="" type="checkbox"/> A FIRST preliminary amendment.  <input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment.</li> <li>14. <input type="checkbox"/> A substitute specification.</li> <li>15. <input type="checkbox"/> Entitlement to small entity status is hereby asserted.</li> <li>16. <input type="checkbox"/> Other items or information:</li> </ol>		

U.S. APPLICATION NO. **09/857569**  
C.F.R. 1.5)INTERNATIONAL APPLICATION NO.  
PCT/JP00/06795ATTORNEY'S DOCKET NUMBER  
10971617. ☒ The following fees are submitted:**Basic National fee (37 CFR 1.492(a)(1)-(5)):**

Search Report has been prepared by the EPO or JPO ....\$860.00

International preliminary examination fee paid to USPTO  
(37 CFR 1.482) .....\$690.00No international preliminary examination fee paid to USPTO  
(37 CFR 1.482) but international search fee paid to USPTO  
(37 CFR 1.445(a)(2)) .....\$710.00Neither international preliminary examination fee (37 CFR  
1.482) nor international search fee (37 CFR 1.445(a)(2))  
paid to USPTO .....\$1,000.00International preliminary examination fee paid to USPTO  
(37 CFR 1.482) and all claims satisfied provisions of PCT  
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☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR  
1.492(e)).

\$

Claims

Number Filed

Number  
Extra

Rate

Total Claims

15 - 20 =

0

X \$ 18.00

\$

Independent Claims

2 - 3 =

0

X \$ 80.00

\$

Multiple dependent claim(s)(if applicable)

+ \$270.00

\$

**TOTAL OF ABOVE CALCULATIONS =**

\$860.00

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**SUBTOTAL =**

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Processing fee of \$130.00 for furnishing the English translation later  
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**TOTAL NATIONAL FEE =**

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- a. ☒ Check No. 119742 in the amount of \$860.00 to cover the above fees is enclosed.
- b. ☐ Please charge my Deposit Account No. \_\_\_\_\_ in the amount of \$\_\_\_\_\_ to cover the above fees. A duplicate copy of this sheet is enclosed.
- c. ☒ The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 15-0461. A duplicate copy of this sheet is enclosed.

**NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.**

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Date: June 7, 2001

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REGISTRATION NUMBER: 30,411

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masatake NAKANO, Kiyoshi MITANI  
and Shinichi TOMIZAWA

Application No.: US National Stage of PCT/JP00/06795

Filed: June 7, 2001

Docket No.: 109716

For: METHOD FOR PRODUCING BONDING WAFER AND BONDING WAFER

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office  
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 1-9 without prejudice to or disclaimer of the subject matter contained therein.

Please add new claims 10-24 as follows:

--10. A method for producing a bonding wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating them at the micro bubble layer as a border, wherein a peripheral portion of a thin film formed on the base wafer is removed after the delamination step.--

--11. The production method according to Claim 10, wherein the thin film has at least an SOI layer.--

--12. The production method according to Claim 10, wherein the removal of the peripheral portion of the thin film is attained by removing a region of 1-5 mm from the peripheral end of the base wafer.--

--13. The production method according to Claim 11, wherein the removal of the peripheral portion of the thin film is attained by removing at least the SOI layer for a region of 1-5 mm from the peripheral end of the base wafer.--

--14. The production method according to Claim 10, wherein the removal of the peripheral portion of the thin film is attained by etching the wafer with masking at least portions of the top surface other than the peripheral portion to be removed.--

--15. The production method according to Claim 12, wherein the removal of the peripheral portion of the thin film is attained by etching the wafer with masking at least portions of the top surface other than the peripheral portion to be removed.--

--16. The production method according to Claim 13, wherein the removal of the peripheral portion of the thin film is attained by etching the wafer with masking at least portions of the top surface other than the peripheral portion to be removed.--

--17. The production method according Claim 10, wherein the removal of the peripheral portion of the thin film is attained by holding together a plurality of wafers stacked so that at least the peripheral portions to be removed should be exposed, and etching them.--

--18. The production method according Claim 12, wherein the removal of the peripheral portion of the thin film is attained by holding together a plurality of wafers stacked so that at least the peripheral portions to be removed should be exposed, and etching them.--

--19. The production method according Claim 13, wherein the removal of the peripheral portion of the thin film is attained by holding together a plurality of wafers stacked so that at least the peripheral portions to be removed should be exposed, and etching them.--

--20. The production method according to Claim 10, wherein the removal of the peripheral portion of the thin film is attained by polishing only the peripheral portion.--

--21. The production method according to Claim 12, wherein the removal of the peripheral portion of the thin film is attained by polishing only the peripheral portion.--

--22. The production method according to Claim 13, wherein the removal of the peripheral portion of the thin film is attained by polishing only the peripheral portion.--

--23. A bonding wafer produced by the hydrogen ion delamination method, wherein a thin film formed on a base wafer is removed for a region of 1-5 mm from a peripheral end of the base wafer.--

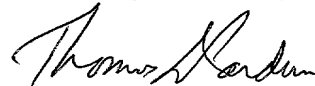
--24. The bonding wafer according to Claim 23, wherein the thin film has an SOI layer and at least the SOI layer is removed for a region of 1-5 mm from the peripheral end of the base wafer.--

REMARKS

Claims 10-24 are pending. Claims 1-9 are cancelled and claims 10-24 are added.

Prompt and favorable consideration on the merits is respectfully requested.

Respectfully submitted,



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WPB:TJP/zmc

Date: June 7, 2001

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09/857569  
JC18 Rec'd PCT/PTO 07 JUN 2001

## SPECIFICATION

### METHOD FOR PRODUCING BONDING WAFER AND BONDING WAFER

#### Technical Field

The present invention relates to a method for producing a bonding wafer by the so-called hydrogen ion delamination method (also called a smart cut method) comprising bonding an ion-implanted wafer to another wafer that serves as a substrate and then delaminating the wafers, which method can reduce failures to be generated in a peripheral portion of the wafer after the delamination.

#### Background Art

As a method for producing an SOI (Silicon On Insulator) wafer using the so-called bonding method, there is known a technique comprising bonding two of silicon wafers via a silicon oxide film, for example, a method comprising forming an oxide film on at least one of such wafers, bonding the wafers to each other without interposing foreign matters between the surfaces to be bonded, and then subjecting them to a heat treatment at a temperature of 200-1200°C to enhance the bonding strength, as disclosed in Japanese Patent Publication (Kokoku) No. 5-46086.

The bonding wafer, of which bonding strength was

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enhanced by such a heat treatment, can be subjected to subsequent grinding and polishing processes.

Therefore, an SOI layer for fabricating elements can be formed by reducing thickness of the wafer on which elements are to be fabricated (bond wafer) to a desired thickness by grinding and polishing.

A bonding SOI wafer produced as described above has advantages of superior crystallinity of SOI layer and high reliability of buried oxide layer existing directly under the SOI layer. However, because it is produced through reduction of thickness by grinding and polishing, the reduction of thickness takes a lot of time and generates waste of the material. In addition, obtainable uniformity of the thickness is only in such a degree of target thickness  $\pm 0.3 \mu\text{m}$  at most.

Further, since there are portions called polishing sag at the peripheral portions of two mirror-surface wafers to be bonded, the portions cannot be bonded and they are left as unbonded portions. If the thickness reduction is performed with existence of such unbonded portions, failures such as delamination of the unbonded portions may be caused during the thickness reduction process. Therefore, these unbonded portions must be removed beforehand (see, for example, Japanese Patent Laid-open (Kokai) Publication No. 3-250616).

Meanwhile, in connection with recent use of higher integration degree and higher processing velocity of semiconductor devices, further reduction to thin film thickness and improvement of film thickness uniformity are required as for the thickness of the SOI layer. Specifically, a film thickness and uniformity represented as  $0.1 \pm 0.01 \mu\text{m}$  or so are required.

Because a thin film SOI wafer having such a film thickness and film thickness uniformity cannot be realized from a bonding wafer by the conventional thickness reduction processing through grinding and polishing, the method called hydrogen ion delamination method was developed as a novel film thickness reduction technique as disclosed in Japanese Patent Laid-open (Kokai) Publication No. 5-211128.

This hydrogen ion delamination method is a technique for producing an SOI wafer, wherein an oxide film is formed on at least one of two silicon wafers, hydrogen ions or rare gas ions are implanted into one wafer (also referred to as bond wafer hereinafter) from its top surface to form a micro bubble layer (enclosed layer) in this silicon wafer, then the ion-implanted surface of the wafer is bonded to the other wafer (also referred to as base wafer hereinafter) via the oxide layer, thereafter the bond wafer is delaminated at the micro bubble layer as a cleavage

plane (delaminating plane) by a heat treatment (delamination heat treatment), and the base wafer on which a silicon layer is formed as a thin film (SOI layer) is further subjected to a heat treatment (bonding heat treatment) to strengthen the bonding to obtain an SOI wafer.

In this hydrogen ion delamination method, it is also possible to directly bond silicon wafers to each other without an oxide film after the ion implantation, and it can be used not only for a case where silicon wafers are bonded to each other, but also for a case where an ion-implanted silicon wafer is bonded to an insulator wafer having a different thermal expansion coefficient such as those of quartz, silicon carbide, alumina and so forth.

By using the hydrogen ion delamination method, the delaminated plane can be obtained as a good mirror surface. Therefore, for example, when an SOI wafer is produced, an SOI wafer having an extremely high uniformity of the SOI layer can be relatively easily obtained. In addition, since the bond wafer after the delamination (also called delaminated wafer hereinafter) can be recycled, the method enjoys an advantage that the material can be used effectively.

Further, since the unbonded peripheral portions are left on the delaminated wafer upon the delamination, it also has an advantage that such a

process of removing the unbonded portions of peripheral portions of wafers as disclosed in the aforementioned Japanese Patent Laid-open (Kokai) Publication No. 3-250616 becomes unnecessary. This is one of the important advantages of the hydrogen ion delamination method including the obtainable film thickness uniformity of SOI layer and the possibility of recycling of the material.

By actually observing a peripheral portion of SOI wafer produced by the hydrogen ion delamination method, it can be seen that the peripheral end of the SOI layer locates in a inside region of about 1 mm from the peripheral end of the base wafer. This is because portions of about 1 mm from the peripheral ends of the bonded two wafers are not bonded due to the polishing sag of the peripheral portions thereof and hence delaminated.

The width of the unbonded portions from the peripheral ends depends on size of the polishing sag, and it is known that it is usually about 1 mm or about 2 mm at most when a usual mirror polished silicon wafer is used.

However, it has become clear that, if an SOI wafer produced by the hydrogen ion delamination method as described above is subjected to various processes such as heat treatment, cleaning and device production, problems may occur including generation of particles

from peripheral portion of the wafer, generation of cracks in the SOI layer and so forth, although occurring frequency is not so high. Because generation of such particles, cracks and so forth may cause reduction of yield or degradation of characteristics in the device production process using SOI wafers, it must be avoided as much as possible.

The cause of the aforementioned generation of particles, cracks and so on is considered as follows. That is, peripheral portions of a bonding wafer produced by the hydrogen ion delamination method do not have unbonded portions and they are physically bonded. However, their bonding strength is not necessarily sufficient compared with the wafer center portions due to the sag in the wafer peripheral portions generated before the bonding. It is considered that, therefore, particles are generated or cracks are formed in the SOI layer from such wafer peripheral portions having insufficient bonding strength during the various heat treatment processes, cleaning process, device production process and so forth after the delamination.

Such a problem is not limited to SOI wafers formed by bonding silicon wafers to each other via an oxide film, but commonly observed in all bonding wafers produced by the hydrogen ion delamination method, for example, the aforementioned SOI wafers

utilizing insulator wafers such as those of quartz, silicon carbide, alumina and so forth as the base wafer, or bonding wafers formed by directly bonding silicon wafers without an oxide film.

#### Disclosure of the Invention

In view of the above problems, an object of the present invention is, when producing a bonding wafer by the hydrogen ion delamination method, to produce a bonding wafer free from the problems of the generation of particles from the peripheral portion of the wafer and the generation of cracks in the SOI layer and so forth.

In order to achieve the aforementioned object, the present invention provides a method for producing a bonding wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating them at the micro bubble layer as a border, wherein a peripheral portion of a thin film formed on the base wafer is removed after the delamination step.

By removing a peripheral portion having insufficient bonding strength of the thin film formed on the base wafer after the delamination step in a method for producing a bonding wafer by the hydrogen

ion delamination method as described above, a bonding wafer having sufficient bonding strength over the whole bonded area can be provided, and thus the problems in a device production process and the like, which are the generation of particles from the peripheral portion of the thin film, the generation of cracks in the thin film and so forth, can be prevented.

The present invention further provides the aforementioned method for producing a bonding wafer in which the thin film has at least an SOI layer.

When the wafer is a bonding SOI wafer in which the thin film formed on the base wafer consists of an SOI layer, or an SOI layer and an insulating film such as an oxide film, at least a peripheral portion of the SOI layer formed on the base wafer can be removed after the delamination step to provide an SOI wafer free from the generation of particles from the peripheral portion of the wafer and the generation of cracks in the SOI layer.

When the peripheral portion of the thin film is removed as described above, it is preferable to remove a region of 1-5 mm from the peripheral end of the base wafer.

Further, when the wafer is a bonding SOI wafer in which the thin film formed on the base wafer has at least an SOI layer, the removal of the peripheral portion of the thin film is preferably attained by

removing at least the SOI layer for a region of 1-5 mm from the peripheral end of the base wafer.

Since the portion showing insufficient bonding strength with respect to the base wafer in the thin film usually exists in such a region, the portion having insufficient bonding strength can be surely removed by forcibly removing that portion of the peripheral portion of the thin film, and thus a bonding wafer in which the whole thin film is firmly bonded to the base wafer can be obtained.

The removal of the peripheral portion of the thin film can be attained by etching the wafer with masking at least portions of the top surface other than the peripheral portion to be removed.

By performing the etching in such a manner as described above, the peripheral portion of the thin film can be easily and surely removed.

Further, as another method, the peripheral portion of the thin film can also be removed by holding together a plurality of wafers stacked so that at least the peripheral portions to be removed should be exposed, and etching them. By such a method, many wafers can be etched simultaneously, and hence the peripheral portion of the thin film can be removed efficiently.

Furthermore, the removal of the peripheral portion of the thin film can be attained by polishing

only the peripheral portion. The peripheral portion of the thin film can also be easily and surely removed by such polishing of only the peripheral portion.

The present invention further provides a bonding wafer produced by the hydrogen ion delamination method, wherein a thin film formed on a base wafer is removed for a region of 1-5 mm from a peripheral end of the base wafer.

Such a bonding wafer can be produced by the aforementioned production method of the present invention, and is free from the problems of the generation of particles from the peripheral portion of the wafer, the generation of cracks in the thin film and so forth.

The present invention also provides the aforementioned bonding wafer, wherein the thin film has an SOI layer and at least the SOI layer is removed for a region of 1-5 mm from the peripheral end of the base wafer.

Such a bonding SOI wafer in which the peripheral portion of the SOI layer is removed for a region of the range from the peripheral end of the base wafer defined above has a film thickness and film thickness uniformity suitable for recent semiconductor devices of high integration degree and high processing velocity. In addition, since the SOI layer is bonded to the base wafer with sufficient bonding strength

over the whole wafer, the problems of the generation of particles from the peripheral portion of the wafer and the generation of cracks in the SOI layer during the device production process and so forth are substantially avoided.

As explained above, according to the present invention, when a bonding wafer is produced by the hydrogen ion delamination method, a peripheral portion of thin film such as SOI layer formed on the base wafer is removed after the delamination step, and thereby a region of insufficient bonding strength can be eliminated and there can be provided a bonding wafer having sufficient bonding strength for the whole wafer.

Such a bonding wafer does not substantially generate particles from the peripheral portion of the thin film and so forth or does not generate cracks in the thin film during subsequent cleaning process, device production process or the like. Therefore, it has advantages of marked reduction of characteristics degradation and improvement of yield.

#### Brief Explanation of the Drawings

Figs. 1 (a) to (h) show a flow diagram of an exemplary process for producing an SOI wafer by the hydrogen ion delamination method according to the present invention.

Fig. 2 is a schematic view illustrating an exemplary method for etching a peripheral portion of thin film of wafer according to the present invention.

Fig. 3 is a schematic view illustrating an exemplary method for removing a peripheral portion of thin film of wafer by polishing according to the present invention.

Fig. 4 is a schematic view illustrating another exemplary method for removing a peripheral portion of thin film of wafer by polishing according to the present invention.

Fig. 5 is a schematic view illustrating another exemplary method for removing a peripheral portion of thin film of wafer by polishing according to the present invention.

Fig. 6 is a schematic view illustrating another exemplary method for removing a peripheral portion of thin film of wafer by polishing according to the present invention.

Fig. 7 is a schematic view illustrating another exemplary method for removing a peripheral portion of thin film of wafer by polishing according to the present invention.

#### Best Mode for Carrying out the Invention

Hereafter, embodiments of the present invention will be explained with reference to the appended

drawings. However, the present invention is not limited to these.

Fig. 1 shows a flow diagram of an exemplary process for producing an SOI wafer, which is an embodiment of bonding wafer, by the hydrogen ion delamination method according to the present invention.

The present invention will be explained hereafter mainly as for a case where two of silicon wafers are bonded via an oxide film to produce an SOI wafer.

In the hydrogen ion delamination method shown in Fig. 1, two mirror-surface silicon wafers are prepared first in the step (a). That is, a base wafer 1 that serves as a substrate and a bond wafer 2 that serves as an SOI layer, which correspond to specifications of devices, are prepared.

Then, in the step (b), at least one of the wafers, the bond wafer 2 in this case, is subjected to thermal oxidation to form an oxide film 3 having a thickness of about 0.1-2.0  $\mu\text{m}$  on its surface.

In the step (c), at least either hydrogen ions or rare gas ions, hydrogen ions in this case, are implanted into one surface of the bond wafer 2 on which surface the oxide film was formed to form a micro bubble layer (enclosed layer) 4 parallel to the surface in mean penetration depth of the ions. The ion implantation temperature is preferably 25-450°C.

The step (d) is a step of superimposing the base wafer 1 on the hydrogen ion implanted surface of the hydrogen ion implanted bond wafer 2 via an oxide film and bonding them. By contacting the surfaces of two of the wafers to each other in a clean atmosphere at an ordinary temperature, the wafers are adhered to each other without using an adhesive or the like.

The subsequent step (e) is a delamination step in which the wafers were delaminated at the enclosed layer 4 as a border to separate them into a delaminated wafer 5 and an SOI wafer 6 in which a SOI layer 7 is formed on the base wafer 1 via the oxide film 3. For example, if the wafers are subjected to a heat treatment at a temperature of about 500°C or more under an inert gas atmosphere, the wafers are separated into the delaminated wafer 5 and the SOI wafer 6 (SOI layer 7 + oxide film 3 + base wafer 1) due to rearrangement of crystals and aggregation of bubbles. In this case, as also shown in Fig. 1, an unbonded portion 8 of peripheral portions of the oxide film 3 and the SOI layer 7 (a region of about 1 mm, or 2 mm at most, from the peripheral end of the base wafer 1) is left on the delaminated wafer 5, and only the portions bonded to the base wafer 1 remain on the base wafer 1 as a thin film 9 (SOI layer 7 + oxide film 3).

The present invention is characterized in that a

peripheral portion of the thin film 9 of which bonding strength with the base wafer 1 is not sufficient, that is, the peripheral portion of the SOI layer 7 or in addition the oxide film 3 in this case, is removed after the delamination step (e). However, since the bonding strength of the wafers obtained in the bonding step (d) and the delamination step (e) as it is would be weak for use in the device production process, the SOI wafer 6 is subjected to a heat treatment at a high temperature as a bonding heat treatment to obtain sufficient bonding strength before the removal. This heat treatment is preferably performed, for example, at 1050°C to 1200°C for 30 minutes to 2 hours under an inert gas atmosphere or an oxidizing gas atmosphere. Such a bonding heat treatment step (f) may be performed after the removal of peripheral portion of the thin film described later, or it may be omitted by increasing the heat treatment temperature of the delamination step (e).

After the bonding heat treatment step (f) is performed in advance as described above as required, the peripheral portion of the thin film 9 of which bonding strength to the base wafer 1 is insufficient, that is, the peripheral portions of the SOI layer 7 or in addition the oxide film 3 in this case, is removed in the step (g) for removing peripheral portion of thin film. The peripheral portion of insufficient





masking tape or the like used for the masking is stripped.

Instead of using a masking tape, it is also possible to coat photoresist on the top surface and expose it to light, so as to mask the top surface other than the peripheral portion. The photoresist is coated on an oxide film after the bonding heat treatment in an oxidizing atmosphere to mask the top surface other than the peripheral portion, and the oxide film of the peripheral portion is removed with hydrofluoric acid. By this treatment, the oxide film is left in the portion masked with the photoresist, and therefore it becomes possible to remove only the peripheral portion of the thin film by performing alkali etching using that oxide film as a mask.

The peripheral portion of the thin film can also be removed by etching a plurality of wafers stacked and held together so that at least the peripheral portions to be removed should be exposed, besides etching a wafer at least of which top surface other than the peripheral portion to be removed is masked as described above.

For example, as shown in Fig. 2, two of SOI wafers 6 stacked so that their SOI layers 7 should face each other are prepared as one set, and a plurality of such sets are stacked by using a columnar jig (not shown in the figure) set at the both ends of

the stacked wafer sets and subjected to etching in that stacked state. In this case, main surfaces of the SOI layers 7 are contacted with each other and hence masked, while the side surfaces (peripheral portions) are exposed to the etching solution 10. Therefore, the SOI layers 7 as well as the oxide films 3 are etched from the side surfaces, and desired regions can be removed.

In the etching operation, the whole wafers may be immersed into an etching solution. However, the etching can surely be attained by exposing to an etching solution only the peripheral portions to be removed or such portions and neighboring portions. Therefore, as shown in Fig. 2, for example, the wafers 6 stacked by using a columnar jig can be rotated so that only the peripheral portions of the wafers 6 should always be in contact with the etching solution 10 by rotating the columnar jig (not shown in the figure).

When wafers stacked as described above are subjected to the etching, spacers may be placed between the wafers, and the aforementioned method of masking portions other than the peripheral portion to be removed by using a masking tape or the like may be used in combination to perform the etching. In such a case, the main surfaces of the SOI layers are surely masked, and they are not etched with etching solution

penetrated from the gaps between the wafers.

By using the method described above, the region of peripheral portion showing insufficient bonding strength can be removed for the SOI layer, and besides the oxide film. However, when the base wafer is a silicon wafer, such a wafer may simultaneously be etched. If it must be prevented, portions of the base wafer to be exposed to the etching solution can be also coated beforehand with the aforementioned masking tape, wax or the like, and then subjected to the etching. Alternatively, if an SOI wafer is produced by using a wafer on which an oxide film is formed beforehand for the whole surface, the oxide film serves as a mask and hence the base wafer is prevented from being etched. However, if the bonding heat treatment (f) shown in Fig. 1 is performed, an oxide film can also be formed on a base wafer, and hence it is also possible to use this oxide film for the above purpose.

As for an SOI wafer, at least a peripheral portion of SOI layer of thin film formed on the base wafer can be removed by performing etching treatment as described above. Thus, an SOI wafer obtained in such a manner does not have peripheral portion of insufficient bonding strength and thus it does not substantially suffer from the problems of generation of particles due to delamination of thin film during

subsequent cleaning step or device production step, generation of cracks in the SOI layer and so forth. Therefore, degradation of characteristics is markedly reduced and the yield is improved.

The peripheral portion of the thin film can also be removed by polishing only the peripheral portion.

Figs. 3-7 are explanatory side views for the cases where the removal of peripheral portion is attained by polishing.

Fig. 3 shows a method of polishing with polishing cloth 23 cut into a circular shape and pressed against a peripheral portion of SOI wafer from above. The SOI wafer 6 is held by a wafer holding table 21 by vacuum suction or the like, and the wafer holding table 21 is rotated by a non-illustrated motor or the like. A turn table 22 adhered with the polishing cloth 23 cut into a circular shape is rotated by a non-illustrated motor or the like around an axis perpendicular to the main surface of the SOI wafer 6 as a center. The end of the polishing cloth 23 is adjusted so that it should locate at a desired distance from the peripheral end of the SOI wafer 6, i.e., 1-5 mm from the peripheral end. Then, polishing is performed with the polishing cloth 23 pressed against the peripheral portion of the SOI wafer 6, while supplying a polishing agent containing colloidal silica and an alkali or an amine as main components to

the peripheral portion of the wafer 6.

Fig. 4 shows a polishing method, wherein a turn table 22 formed in a cup-like shape is adhered with a ring-like polishing cloth 23 having an inner periphery (inner diameter) at a distance of 1-5 mm from the peripheral end of the SOI wafer 6, that is, having an inner diameter smaller than the diameter of the base wafer by 2-10 mm and an outer diameter equal to the diameter of the base wafer or larger than it, and polishing is performed by pressing the polishing cloth from above against the peripheral portion of the SOI wafer 6 with aligning the rotation axis of the turn table 22 with that of the SOI wafer 6.

Fig. 5 shows a polishing method, wherein polishing is performed by pressing an end portion of polishing cloth (buff) 23 cut into a circular shape or having a cylindrical shape with a small thickness against the peripheral portion of the SOI wafer 6 from above or side with rotation around an axis parallel to the main surface of the SOI wafer 6 as a center.

Fig. 6 shows a polishing method, wherein polishing is performed by pressing polishing cloth (buff) 23 having a cylindrical shape against the peripheral portion of the SOI wafer 6 from above with rotation around an axis parallel to the main surface of the SOI wafer 6 as a center.

Fig. 7 shows a polishing method, wherein

polishing is performed with polishing cloth (buff) 23 having a cylindrical shape and a groove 24 of a desired depth on its side surface by pressing an upper surface of the groove 24 against the peripheral portion of the SOI wafer 6 with rotation of the cylindrical polishing cloth 23 around an axis perpendicular to the main surface of the SOI wafer 6 as a center.

The polishing cloth may consist of polyurethane foam, nonwoven fabric impregnated with polyurethane or the like, which is usually used for the polishing of silicon wafers.

As for the polishing, since the alkali or amine contained in the polishing agent has an action of etching silicon, the polishing agent is preferably supplied to only the peripheral portion as much as possible. In order to prevent the polishing agent from being brought into contact with portions other than the peripheral portion, it is also possible to supply pure water to the center of the wafer so that the pure water should cover the portions other than the peripheral portion with the aid of centrifugal force.

In the aforementioned embodiments, the present invention is explained for an SOI wafer that uses two of silicon wafers in which an SOI layer is formed on one of the silicon wafers (base wafer) via an oxide

film. However, the present invention is not limited to it, and it can be applied to all bonding wafers produced by the hydrogen ion delamination method.

As described above, for example, in an SOI wafer consisting of a silicon wafer (bond wafer) implanted with ions and bonded to an insulator wafer (base wafer) having a different thermal expansion coefficient such as those of quartz, silicon carbide, alumina and so forth, a thin silicon layer (SOI layer) is formed on the insulator wafer. Also in such a wafer, a region showing insufficient bonding strength is present in a peripheral portion of the SOI layer after the delamination heat treatment. Therefore, by removing the peripheral portion, specifically, a region of 1-5 mm from the peripheral end of the base wafer, there can be obtained an SOI wafer in which the SOI layer is firmly bonded to the insulator wafer over the whole wafer.

Further, in a case of bonding wafer obtained by directly bonding silicon wafers to each other without an oxide film, a thin silicon layer is formed on the silicon wafer. Also in such a case, the region of insufficient bonding strength in the peripheral portion of the silicon layer can be removed according to the present invention to leave only the portion of the silicon layer firmly bonded to the silicon wafer for the whole wafer. Thus, generation of particles

from the peripheral portion of the wafer, generation of cracks in SOI layer during subsequent cleaning step, device production step and so forth can be prevented.

For any of the aforementioned bonding wafers produced by the hydrogen ion delamination method, the peripheral portion of the thin layer formed on the base wafer can be removed by etching the bonding wafer with masking at least the top surface area other than the peripheral portion to be removed, or etching a plurality of bonding wafers stacked and held in one piece so that at least peripheral portions to be removed should be exposed as described above. Furthermore, the peripheral portion of the thin layer may be removed by polishing only the peripheral portion.

The present invention is not limited to the embodiments described above. The above-described embodiments are mere examples, and those having the substantially same structure as that described in the appended claims and providing the similar functions and advantages are included in the scope of the present invention.

## CLAIMS

1. A method for producing a bonding wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating them at the micro bubble layer as a border, wherein a peripheral portion of a thin film formed on the base wafer is removed after the delamination step.
2. The production method according to Claim 1, wherein the thin film has at least an SOI layer.
3. The production method according to Claim 1 or 2, wherein the removal of the peripheral portion of the thin film is attained by removing a region of 1-5 mm from the peripheral end of the base wafer.
4. The production method according to Claim 2, wherein the removal of the peripheral portion of the thin film is attained by removing at least the SOI layer for a region of 1-5 mm from the peripheral end of the base wafer.
5. The production method according to any one of Claims 1-4, wherein the removal of the peripheral

portion of the thin film is attained by etching the wafer with masking at least portions of the top surface other than the peripheral portion to be removed.

6. The production method according to any one of Claims 1-5, wherein the removal of the peripheral portion of the thin film is attained by holding together a plurality of wafers stacked so that at least the peripheral portions to be removed should be exposed, and etching them.

7. The production method according to any one of Claims 1-4, wherein the removal of the peripheral portion of the thin film is attained by polishing only the peripheral portion.

8. A bonding wafer produced by the hydrogen ion delamination method, wherein a thin film formed on a base wafer is removed for a region of 1-5 mm from a peripheral end of the base wafer.

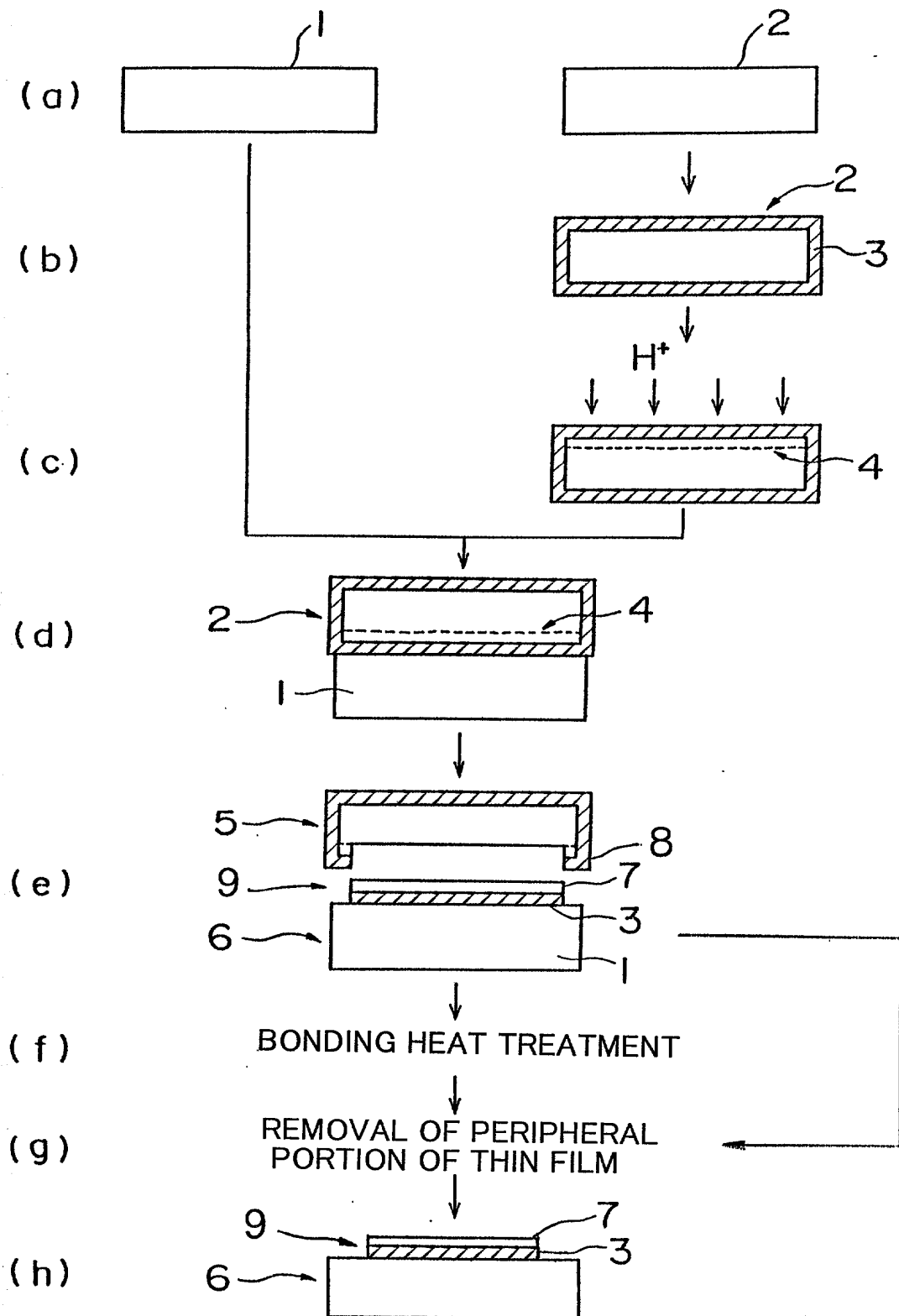
9. The bonding wafer according to Claim 8, wherein the thin film has an SOI layer and at least the SOI layer is removed for a region of 1-5 mm from the peripheral end of the base wafer.

## ABSTRACT

In a method for producing a bonding wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating them at the micro bubble layer as a border, a peripheral portion of a thin film formed on the base wafer is removed after the delamination step. Preferably, a region of 1-5 mm from the peripheral end of the base wafer is removed. In the production of a bonding wafer by the hydrogen ion delamination method, there can be provided a bonding wafer free from problems such as generation of particles from peripheral portion of the wafer and generation of cracks in the SOI layer.

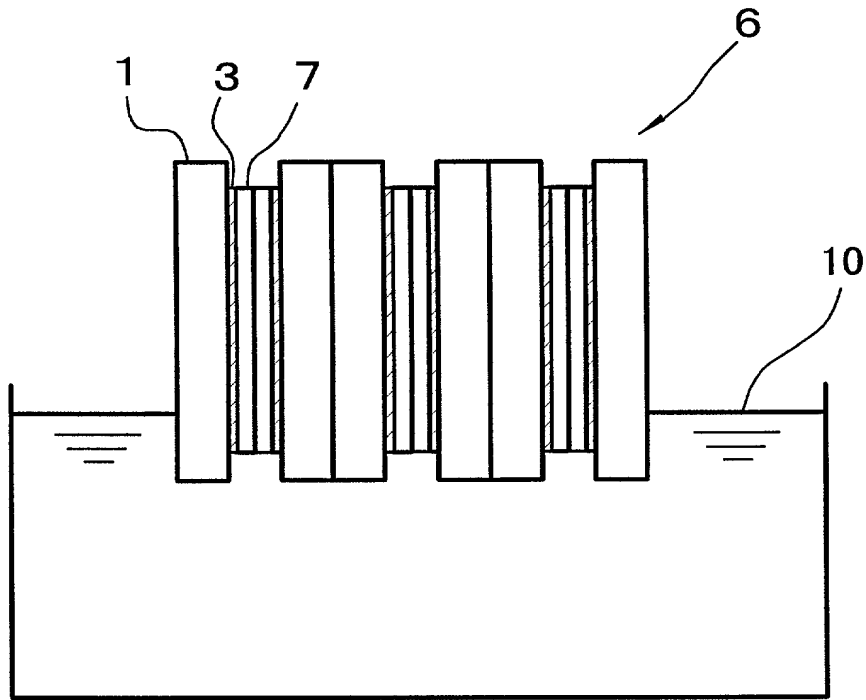
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FIG. 1



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FIG. 2



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FIG. 3

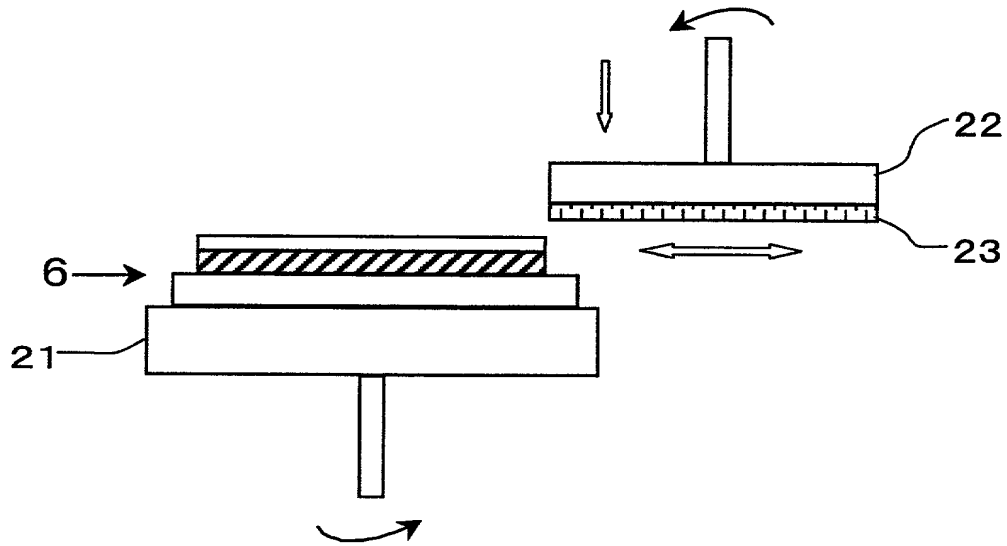
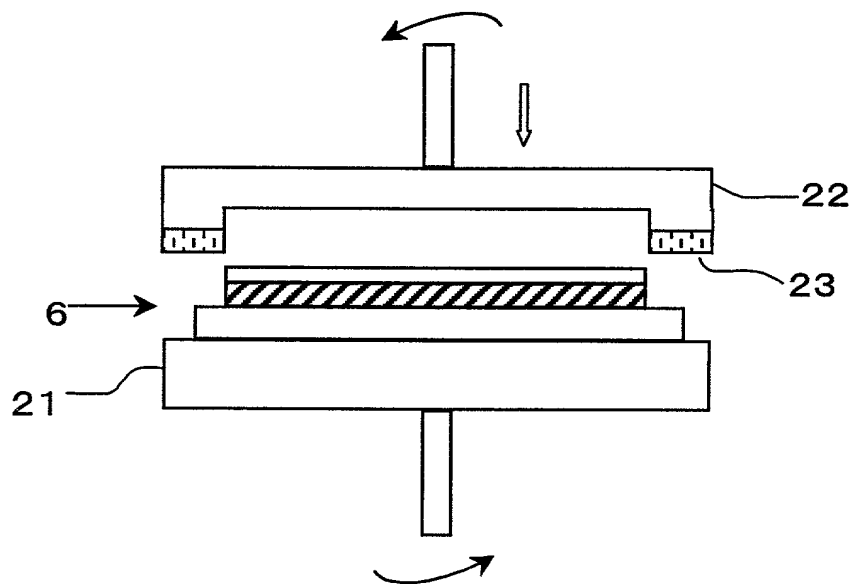


FIG. 4



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FIG. 5

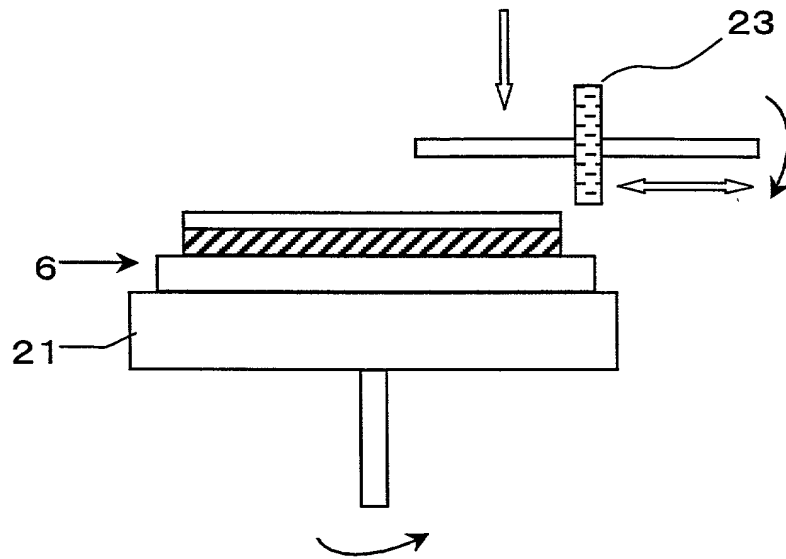


FIG. 6

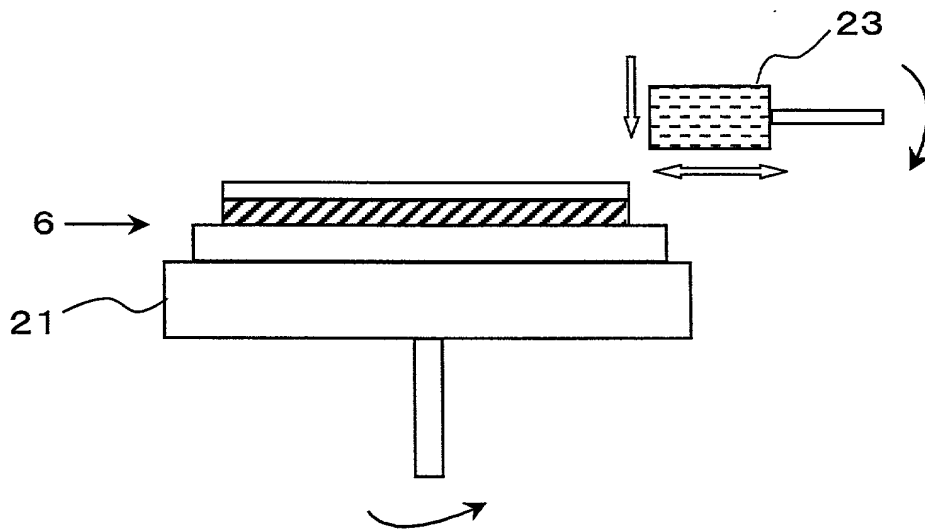
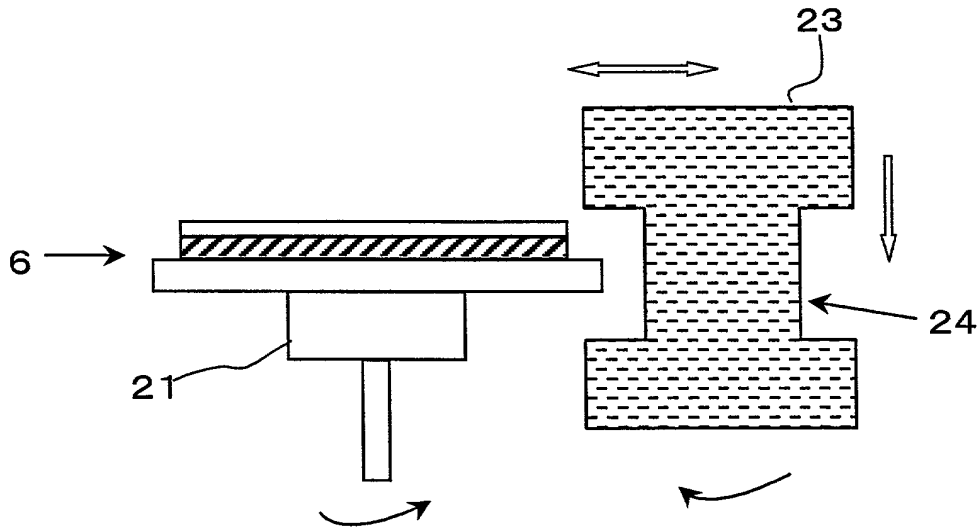


FIG. 7



# Declaration and Power of Attorney for Patent Application

## 特許出願宣言書兼委任状

### Japanese Language Declaration

私は、下欄に氏名を記載した発明者として、以下のとおり宣言する：

私の住所、郵便宛先および国籍は、下欄に氏名に続いて記載したとおりであり、下記名称の発明に関し、特許請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR PRODUCING BONDING WAFER AND BONDING WAFER

その明細書を  
(該当するものにチェック)  
☐ ここに添付する。

☒ 2000 年 9 月 29 日に

出願番号第 PCT/JP00/06795 として提出され、

\_\_\_\_ 年 \_\_\_\_ 月 \_\_\_\_ 日に補正し、  
(該当する場合)

私は、前記のとおり補正した特許請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

私は、連邦施行規則第 37 章第 1 条第 56 項に従い、本願の特許性の有無について重要な情報を開示すべき義務を有することを認める。

私は、米国法第 35 章第 119 条に基づく下記の外国特許出願もしくは発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の提出日前の提出日を有する外国特許出願もしくは発明者証出願および/もしくは米国仮出願を以下に明記する：

the specification of which  
(check one)

☐ is attached hereto.

☒ was filed on September 29, 2000 as

Application Serial No. PCT/JP00/06795

and was amended on \_\_\_\_\_  
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and/or any U.S. provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior foreign and/or provisional applications  
先行外国出願/仮出願

Priority claimed  
優先権の主張

11-292130 (Number/番号)	Japan (Country/国名)	14 October 1999 (Day/Month/Year Filed/提出年月日)	<input checked="" type="checkbox"/> (Yes/はい)	<input type="checkbox"/> (No/いいえ)
_____ (Number/番号)	_____ (Country/国名)	_____ (Day/Month/Year Filed/提出年月日)	<input type="checkbox"/> (Yes/はい)	<input type="checkbox"/> (No/いいえ)
_____ (Number/番号)	_____ (Country/国名)	_____ (Day/Month/Year Filed/提出年月日)	<input type="checkbox"/> (Yes/はい)	<input type="checkbox"/> (No/いいえ)
_____ (Number/番号)	_____ (Country/国名)	_____ (Day/Month/Year Filed/提出年月日)	<input type="checkbox"/> (Yes/はい)	<input type="checkbox"/> (No/いいえ)

私は、米国法第 35 章第 120 条に基づく下記の米国特許出願の利益を主張し、本願の特許請求の範囲各項に記載の主題が米国法第 35 章第 112 条の第 1 段落に規定の態様で先の米国出願に開示されていない限度において、先の出願の提出日と本願の国内提出日もしくは P C T 国際出願提出日の間に公表された連邦施行規則第 37 章第 1 条第 56 項に記載の重要な情報を開示すべき義務を有することを認める。

I hereby claim the benefit under Title 35, United States code, §120 of any United States application(s) listed below and, in so far as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112. I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

_____ (Application Serial No./出願番号)	_____ (Filing Date/提出日)	_____ (Status: Patented, Pending, abandoned/ 現状：特許成立、係属中、放棄済み)
_____ (Application Serial No./出願番号)	_____ (Filing Date/提出日)	_____ (Status: Patented, Pending, abandoned/ 現状：特許成立、係属中、放棄済み)

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従って行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、米国法第 18 章第 1001 条により、罰金もしくは禁錮に処せられるか、またはこれらの刑が併科され、またかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損なうことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true: and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Citizenship/国籍	
Post Office Address/郵便宛先	
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Residence/住所	
Citizenship/国籍	
Post Office Address/郵便宛先	
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Residence/住所	
Citizenship/国籍	
Post Office Address/郵便宛先	

Supply similar information and signature for seventh and subsequent joint inventors.  
第七又はそれ以降の共同発明者に対しても同様の情報および署名を提供すること。

委任状：私は下記発明者として、以下の代理人をここに選任し、本願の手続を遂行すること並びにこれに関する一切の行為の特許商標庁に対して行うことを委任する。(代理人氏名および登録番号を明記のこと)

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

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Inventor's signature/同発明者の署名 <u>Masatake Nakano</u>	Date/日付 <u>April 16, 2001</u>
Residence/住所 <u>Gunma Japan JPX</u>	
Citizenship/国籍 <u>Japanese</u>	
Post Office Address/郵便宛先 <u>c/o Shin-Etsu Handotai Co., Ltd. Isobe R&amp;D Center</u> <u>13-1, Isobe 2-chome, Annaka-shi, Gunma 379-0196 Japan</u>	
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